L Number	Hits	Search Text	DB	Time stamp
1	3	6223326.pn. 5995736.pn. 5673199.pn.	USPAT	2003/05/07 16:28
-	18	(FIELDS-CAROL-A FIELDS-CARLO WILLIAMS-ANTHONY-D WILLIAMS-ANTHONY).in.	USPAT; EPO; JPO; IBM_TDB	2003/05/06 11:15
-	11	(seltzer fulton patel-dhimant kumar-veena).in. and xilinx.as.	USPAT; EPO; JPO; IBM_TDB	2003/05/02 15:43
-	1	6002861.pn.	USPAT; EPO; JPO; IBM_TDB	2003/05/02 15:56
-	1	"4697241".PN.	USPAT	2003/05/02 21:00
-	1	"4751637".PN.	USPAT	2003/05/02 15:56
-	1	"4775950".PN.	USPAT	2003/05/02 15:56
-	114	703/16.ccls.	USPAT; EPO; JPO; IBM_TDB	2003/05/02 15:56
-	28723	(hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:15
-	11381	((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	11104	(((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	2840	((((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	687	(((((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	621	((((((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:18
-	243	(((((((hardware same logic same simulator) or (VHDL or HDL or (schematic adj c) or ASIC or FPGA)) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:18
-	423	(VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17

-	274	((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	274	(((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:17
-	145	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:30
-	103	(((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:29
-	100	((((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:18
-	72	(((((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect$3 or locat$3 or find$3)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:19
-	72	((((((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property))) and (hierarchy or hierarchical)) and (store or storage or database)) and (debug or debugging or (error same (detect$3 or locat$3 or find$3)))) and (link$3 or connect$3 or associat$3)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:29

-	145	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:31
-	0	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link$3 or connect$3 or associat$3) same (simulation with (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:34
-	2	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link$3 or connect$3 or associat$3) same (simulat$3 same (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:35
-	6	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link$3 or connect$3 or associat$3) same ((simulat$3 or test$3) same (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:38
-	60	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat$3) or (logic same simulat$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link$3 or connect$3 or associat$3))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:08
-	102	(VHDL) and (high adj level) and (physical adj implementation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:10

-	0	(VHDL) and ((high adj level) same (physical adj implementation)) same ((data adj base) or (database))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:11
-	77	((VHDL) and (high adj level) and (physical adj implementation)) and database	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:11
-	2	(((VHDL) and (high adj level) and (physical adj implementation)) and database) and testbench	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:11
-	3	object same oriented same VHDL same database	USPAT; EPO; JPO; IBM_TDB	2003/05/06 13:43
-	223	(rostocher).in. OR (dangelo).in.	USPAT; EPO; JPO; IBM_TDB	2003/05/06 13:45
-	8	(hierarch$4 or generation$2 or tree or child$3) same VHDL same database	USPAT; EPO; JPO; IBM_TDB	2003/05/06 13:45